Prateek P. Kulkarni

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Last Updated in September 2026.

Research Interests

My research revolves around co-designing **compilers, runtime schedulers and architecture** for **quantum systems** that are correct, efficient, and deployable at scale. My recent focus has been **resource utilization and allocation** in quantum computers across different abstraction layers. Going ahead, I intend to work on problems in compilation for the **fault-tolerant quantum computing** paradigm.

Education

B. Tech. **PES University**, Electronics and Communication Engineering — Bangalore, India
Major Project: Quantum Machine Learning on Photonic Processors. — 2022 – 2026

Research Visits

The Fields Institute, Visiting Researcher — Toronto, Canada
Thematic Program on Quantum Algorithms for Differential Equations. — October – December 2026

Publications

Synthesizing Logical Clifford Representations for Subsystem Codes via Parallel Search.
Prateek P. Kulkarni, Narayanan Rengaswamy
Submitted to 39th ACM Symposium on Parallelism in Algorithms and Architectures **(SPAA 2027)**
Brief Announcement (Under Review)

How Many Shots Does It Take? A Noise-Aware Quantum Resource Allocation Framework.
Prateek P. Kulkarni, Sumit K. Mandal
Proceedings of 31st ACM/IEEE Int'l Symposium on Low Power Electronics and Design **(ISLPED 2026)**
Extended Version Invited to **IEEE TVLSI** [arXiv:2607.24704]

AutoQuREO: An Automated Framework for Quantum Resource Estimation and Optimization.
Harshkumar Oza, Aritra Sarkar, Syed Naqi Abbas, Rahul Bhowmick, Aryan Prakash, **Prateek P. Kulkarni**, Krishna Kumar Sabapathy
Preprint 2026; Contributed Talk, PLanQC at POPL 2027 [arXiv:2608.12936]

Research Experience

Indian Institute of Science, Walmart Predoctoral Fellow — Bangalore, India
Advisor: Prof. Sumit K. Mandal, Dept. of CSA — July 2026 – Present

- Built a runtime scheduling framework for multi-tenant quantum systems that aims to jointly optimize qubit placement & circuit execution timing to reduce inter-circuit crosstalk on shared quantum hardware.
- Designed a hybrid heuristic–SMT scheduler achieving up to **2.75**× fidelity improvement and **1.9**× throughput gain over state-of-the-art baselines on real quantum devices, with $<$ **2%** runtime overhead.

University of Cambridge, Research Assistant — Remote
Advisor: Prof. Prakash Murali, Dept. of CS — March – July 2026

- Designed a compiler abstraction for efficient embedding of qLDPC codes (Gross family) onto constant-degree coupling maps, via graph factorization, compatible with present-day hardware.
- Achieved up to **60%** reduction in coupling degree and up to **3.5**× shorter long-range couplers over state-of-the-art baselines (with provably-optimal bounds).

Fujitsu Research India, Research Intern — Bangalore, India
Advisors: Dr. Aritra Sarkar and Harshkumar Oza, Quantum Lab — April – June 2026

- Developed compilation adapters and resource estimation models targeted at early fault-tolerant paradigm, for AutoQuREO, a proprietary quantum optimization framework, enabling the automated analysis of quantum algorithms and identifying circuit-level optimizations to reduce execution overhead.

Indian Institute of Science, Research Intern — Bangalore, India
Advisor: Prof. Sumit K. Mandal, Dept. of CSA — Summer 2024, Summer & Fall 2025

Hardware-Aware Resource Allocation for Noisy Quantum Devices (ISLPED 2026):

- Developed analytical models relating shot count to success probability, circuit partitioning, and resource allocation in noisy settings; >**95%** accuracy on real quantum devices.
- Proposed a variance-aware shot allocation strategy that reduces estimation error by **63%**, over-provisioned shots by **58%**, and energy consumption by **60%** across benchmarks.

Coupling Map Design via Spectral Graph Theory (3rd Prize, ACM SRC at MICRO 2025):

- Built analytical models estimating the quantum processor fidelity and execution time from coupling maps and hardware constraints; > **98%** accuracy on real devices.
- Designed an efficient (polynomial-time) coupling map generation algorithm exploiting the spectral graph structure, improving circuit fidelity by up to **35%**.

Selected Talks and Poster

Invited Talk, Rethinking Resource Allocation on Noisy Quantum Computers — QuCS, September 2026

Poster, Entanglement-dependent Error Bounds for Hamiltonian Simulation — ECCC, TQC 2026

Selected Projects

StencilQ: Crossbar-Free FPGA Dataflow for qLDPC Decoding

- Developed a compiler-driven FPGA architecture that exploits the spacetime structure of qLDPC syndrome circuits to replace generic crossbar-based communication with static permutation schedules.
- Reduced over **51k** routing interactions to just **129** reusable route templates for the Gross $[[144, 12, 12]]$ code, enabling a **7-stage** torus permutation network with no BRAM or DSP overhead.

Subsystem Logical Clifford Synthesis

with Prof. Narayanan Rengaswamy, University of Arizona

- Developed a randomized synthesis framework for subsystem-code Clifford circuits that exploits gauge freedom to efficiently search over logically equivalent implementations under hardware constraints.
- Combined algebraic generation with property-tested filtering to avoid exhaustive enumeration, achieving up to **3.65**× parallel speedup and **43.6%** lower estimated nonlocal infidelity on Bacon–Shor code instances.

Relevant Technical Skills

- **Languages:** Python, Matlab, (some) L∃∀N
- **Platforms and Tools**: Qiskit, Cirq, CUDA-Q, Stim, Qualtran, Quimb, QuTiP.

Academic Service

- **Reviewing:** IEEE TQE 2025, ISLPED 2026, ICML AI4Math Workshop 2026
- **Artifact Evaluator**: POPL 2027, SOSP 2026, HPCA 2026
- **Teaching Assistant:** Quantum Transport and Logic Gates, PES University, 2025.

Awards and Honors

- **3rd Prize**, ACM Student Research Competition at **MICRO 2025**, Undergraduate Category.
- **SPARKS Predoctoral Research Fellowship 2025**, Dept. of CSA, IISc, 1/5 positions nationally.
- **Indian National Academy of Engineering (INAE) Mentee 2026**, 1/60 positions nationally.