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SELECTED PROJECTS	<b>PipSim: Real-Time RISC-V Pipeline Simulator with Visualization for Instruction Hazards</b> <i>Github Repository</i> 2025.02 – 2025.02	
	<ul style="list-style-type: none"> <li>Developed a Python-based simulator with real-time visualization of instruction flow, hazards, and pipeline behavior for 5-stage RISC-V.</li> <li>Integrated data forwarding and branch prediction; Currently extending with advanced features such as superscalar execution and deeper pipeline support.</li> </ul>	
	<b>RegDyno.Ai: High-Accuracy Time-Series Prediction using Custom Distribution Modeling</b> <i>Patent Published, Journal No. 1/2025</i> 2023.12 – 2024.06	
	<ul style="list-style-type: none"> <li>Built a custom distribution-based model achieving 15–25% improvement over state-of-the-art forecasting methods (ARIMA, LSTM, Prophet).</li> <li>Deployed a production-ready pipeline with automated noise reduction; novel methodology led to patent publication.</li> </ul>	
	<b>surface2cirqit: Automated Surface Code to Quantum Circuit Conversion with Optimization</b> <i>Github Repository</i> 2024.06 – 2024.08	
	<ul style="list-style-type: none"> <li>Created an automated pipeline for Surface Code to Quantum Circuit conversion with syndrome extraction and optimization.</li> <li>Reduced gate count by 20–40% and enabled seamless integration with Qiskit, Cirq, and other error correction frameworks.</li> </ul>	
SKILLS	<b>Programming:</b> Python, Julia, C, MATLAB.	
	<b>Tools/Platforms:</b> Vivado, gem5, Qiskit, QuNetSim, Cirq, PennyLane. <b>Languages:</b> English, Kannada, Hindi	
SELECTED TALKS	<b>Systems Day 2025</b>   Computer Science and Automation, IISc 2025.01 <ul style="list-style-type: none"> <li>Selected among ~20 researchers nationwide to present a poster; presented on multi-core quantum computing with superconducting qubits.</li> </ul>	
	<b>Workshop on Automata and Games for Synthesis</b>   45th FSTTCS 2025.12 <ul style="list-style-type: none"> <li>Selected to present a short talk on: <i>Quantum Communication Exponentially Speeds-up Circuit Synthesis</i></li> </ul>	
AWARDS AND HONORS	<ul style="list-style-type: none"> <li><b>Pre-Doctoral Fellowship</b>, SPARKS Programme, CSA, IISc (~1/4 positions) 2025.10</li> <li><b>3rd Place Globally</b>, ACM SRC at MICRO 2025, UG Category 2025.10</li> <li><b>Student Travel Grant</b>, MICRO 2025 – \$580 for ACM SRC presentation 2025.09</li> <li><b>Q-Pragathi Funding</b>, KITS, Govt. of Karnataka – 1.2L INR 2024.09</li> <li><b>Funded Internship</b>, ISFCR Long-Term Internship (declined), PES University 2024.01</li> <li><b>National Runner-up</b>, Explain The Concept, Pravega (Undergrad Fest), IISc 2019.02</li> </ul>	
	<b>Teaching Assistant for:</b> <i>Quantum Transport and Logic Gates</i> , <i>PES University, Spring 2025, (Credits: 4, Class size: ~90)</i>	
	<b>Program Committee for:</b> <i>HPCA 2026 - AE (Artifact Evaluation)</i>	
	<b>Reviewer for:</b> <i>IEEE Transactions on Quantum Engineering (TQE)</i>	
REFERENCES	<b>Prof. Sumit K. Mandal</b> Assistant Professor, Dept. of CSA Indian Institute of Science (IISc), Bangalore Email: skmandal@iisc.ac.in	<b>Prof. Kaustav Bhowmick</b> Associate Professor, Dept. of ECE PES University, Bangalore Email: kaustavbhowmick@pes.edu